REMARKS

Claims 12-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lien et al (U.S. Pat. No. 6,211,851, herein after "Lien").

Claims 1-4, 7-9, 11, and 15-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Pat. Pub. 2002/0075214) in view of Lien.

Claim 5 is rejected under 35 USC § 103(a) as being unpatentable over Kim and Lien and further in view of Washio.

Claim 6 is rejected under 35 USC § 103(a) as being unpatentable over Kim and Lien and further in view of Lautzenhizer.

Claim 10 is rejected under 35 USC § 103(a) as being unpatentable over Kim and Lien and further in view of AAPA.

The rejections are respectfully traversed in light of the following remarks, and reconsideration is requested.

Amendments to the Specification

The specification has been amended to correct clerical errors. In particular, the paragraph beginning on page 9, line 15, has been amended to replace "SW2 is turned on and SW2 is turned off" to "SW1 is turned on and SW2 is turned off". This amendment is supported at least by Fig. 3, which shows the states of SW1 and SW2.

Rejections under 35 U.S.C. § 102(b)

Claims 12-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lien et al (U.S. Pat. No. 6,211,851, herein after "Lien").

Claim 12 is amended to recite, in part, as follows:

> receiving the first data voltage from the data line and storing in a capacitor the first data voltage during the scanning of the first gate line;
> scanning the second gate line;
> applying the stored first data voltage from the capacitor_to the data line during the scanning of the second gate line; and
> applying a second data voltage to the data line during the scanning of the second gate line.

No new matter is added. Support for the amendment is found in the specification at least in paragraph [0022].

Lien fails to teach or suggest the claimed method. Lien describes providing a serial data signal from a frame buffer as follows:

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> Serial data by row which for example could be provided from a frame buffer (not shown) is provided via data input line 2 to the first input of an analog toggle 4 and to the input of an inverter 6. The serial data on line 2 is provided twice so that the output of the toggle switch 4 is the serial signal A equal to D1,-D1,D2,-D2,D3,-D3, etc., where D1 represents the serial data V1 through VK at time t...
>
> (Col. 5, lines 40-47; emphasis added.)

Lien does not teach or suggest applying a stored first data voltage from a capacitor to the data line during the scanning of the second gate line, and applying a second data voltage to the data line during the scanning of the second gate line. Thus, Lien does not anticipate the method recited in claim 12.

Since Lien fails to teach or suggest each every element of claim 12 (as amended) and claims 13-14 depend from independent claim 12, Applicants respectfully request that the rejection under 35 U.S.C. § 102(b) in view of Lien be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 1-4, 7-9, 11, and 15-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Pat. Pub. 2002/0075214) in view of Lien.

Concerning claim 1, Examiner states on page 4 that Kim teaches "a master data driver ("master column driver 220") sequentially applying data voltages selected from the gray voltages corresponding to the image data to the data line, each application is performed in the second period [par. (0051) lines 1-5] [figs. 4 and 7]; and a slave data driver ("slave column driver 230") *applying a pre-charging/compensation voltage to the data line in each first period* [par. (0051) lines 5-8] [figs. 4 and 7]." (Emphasis added).

Applicants respectfully traverse the Examiner's rejection. Claim 1 is amended to recite, in part:

> a master data driver sequentially applying to the data line data voltages selected from the gray voltages corresponding to the image data, wherein each application is performed in the second period of a present horizontal period; and
> a slave data driver storing the data voltage applied to the data line in the second period of the present horizontal period and applying the stored data voltage to the data line in the first period of a next horizontal period.

No new matter is added. Support for the amendments is found in at least paragraphs [0044] – [0047] and Fig. 3.

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Kim fails to teach or suggest a slave data driver storing the data voltage applied to the data line in the second period of the present horizontal period and applying the stored data voltage to the data line in the first period of a next horizontal period, as recited in claim 1. Kim describes the slave control unit 540, in part:

> [0048] The slave control unit 540 operates by receiving the control signals generated by the timing controller, which is installed in the master PCB 200. The slave control unit 540 outputs control signals at predetermined times such that the on/off switch 510 shorts or opens, and the three-state buffer converter 520 *selects one of the three voltages*. It is also possible for the control signals used to operate the on/off switch 510 and the *three-state buffer converter* 520 to be directly generated in the timing controller of the master PCB 200. The predetermined times at which the control signals are output, refer to the output of the control signals at times suitable for the resolution of the flat panel display according to polarity signals 541, which control polarity, and load signals 542, which enable D/A conversion and transmission.
>
> (Emphasis added.)

In other words, Kim merely teaches the selection of one of three voltages from the buffer converter 520. In contrast, claim 1 recites that the slave driver *stores* the data voltage applied to the data line in the second period of the present horizontal period and *applies* the *stored* data voltage to the data line in the first period of a next horizontal period.

Lien fails to cure the deficiencies of Kim. In particular, Lien does not teach or suggest a method of using a master data driver and a slave data driver. Instead, Lien describes:

> "For every gate driver output signal duration, represented by T, the data driver shift register parallel output (from 1 to M) is composed of the crosstalk compensation signal during a first portion of T and then followed by the unadulterated data signal (no compensation) during the remaining portion of T, as shown in the waveform timing diagram of FIG. 2(f)."
> [Lien: col. 6, lines 13-19]

Neither Kim nor Lien teach or suggest all of the limitations recited in claim 1. Accordingly, the Examiner has not established a *prima facie* case of obviousness of claim 1. Applicants respectfully request withdrawal of the rejection under § 103 of claim 1 and claims 2-4, 7-9, and 11, which depend from claim 1.

Claim 15 has been rejected on the same basis as claims 1 and 12. Claim 15 recites, in part: "a slave data driver storing the first data voltages in the first period and applying the stored first data voltage to the data line in the second period." For at least the reasons given above with respect to claim 1, Applicants submit that the Examiner has not established a *prima facie* case of obviousness of claim 15. Therefore, Applicants respectfully request withdrawal of the rejections of claim 15 and claims 16-19, which depend from claim 15. Accordingly, Applicants respectfully request that the Examiner withdraw the rejections under 35 U.S.C. § 103(a) of claims 1-4, 7-9, 11, and 15-19.

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Claim 5 stands rejected under 35 USC § 103(a) as being unpatentable over Kim and Lien and further in view of Washio. Washio fails to cure the deficiencies of Kim and Lien, as described above.

Therefore, the Examiner's rejection of claim 5 is unsupported and withdrawal of the rejection is requested.

Claim 6 stands rejected under 35 USC § 103(a) as being unpatentable over Kim and Lien and further in view of Lautzenhizer. Lautzenhizer fails to cure the deficiencies of Kim and Lien, as described above. Therefore, the Examiner's rejection of claim 6 is unsupported and withdrawal of the rejection is requested.

Claim 10 stands rejected under 35 USC § 103(a) as being unpatentable over Kim and Lien and further in view of AAPA. The AAPA fails to cure the deficiencies of Kim and Lien, as described above. Therefore, the Examiner's rejection of claim 10 is unsupported and withdrawal of the rejection is requested.

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CONCLUSION

Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is kindly solicited.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time and/or fee for additional claims, which may be required.

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Certificate of Transmission: I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's electronic filing system on Feb 27 2007.

Attorney for Applicant(s) — Date of Signature: 2/27/2007

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